1. The state diagram of a sequential circuit is given as below. (30 Marks)

   a. Tabulate the related state table.

   4 Marks

   b. Reduce the state table to a minimum number of states using row matching.

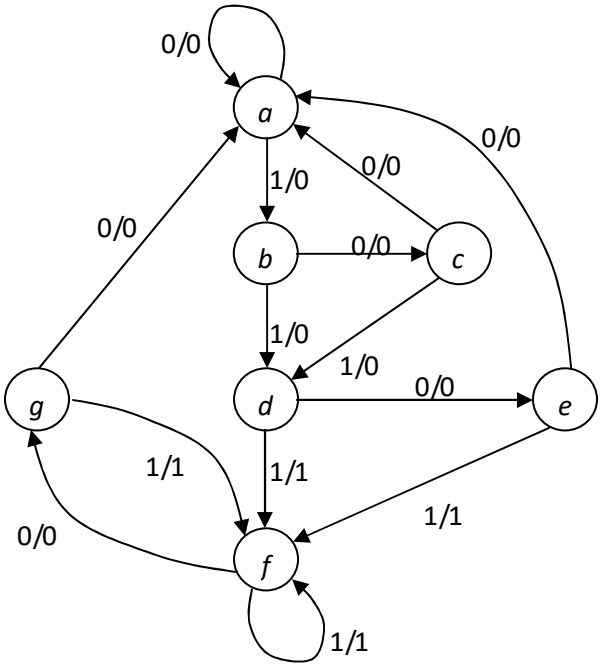
   10 Marks

   c. Repeat b) using an implication table. Please provide the complete steps involved in using the table.

   10 Marks

   d. Draw the reduced state diagram.

   6 Marks



2. We are interested to design a 3-bit counter which counts in the following sequence: (45 Marks)

001, 011, 010, 110, 111, 101, 001..

(a) Identify all the steps required if you are asked to design three sequential circuits to implement the counter using:

   a. Clocked D flip flops (10 Marks)
   b. Clocked T flip flops (10 Marks)
   c. Clocked J-K flip flops (10 Marks)

(b) For each of the above, use MULTISIM to show the performance of the circuit.

15 Marks

3. Solve the following problems on VHDL (25 Marks)

   a. Design using the VHDL system to model a MOORE finite state machine that acts as a “1011” sequence detector. Your design should detect overlapping sequences. Assume the input is named **A**, the output is named **Z** and that an active low reset signal (**reset_n**) asynchronously resets the machine. Implement positive edge triggered flip-flops.

      i. Draw the MOORE model state diagram for the FSM
      5 Marks

      ii. Write the complete VHDL construct to implement the FSM
      10 Marks

   b. Write a VHDL description for a 4-bit shift register. The shift register is to be negative edge triggered. **Sin** is a serial input to the most significant bit of the shift register. **Sout** is a serial output from the least significant bit of the shift register. **En_n** is an active low enable. **sreg** is the 4-bit register. Write only the VHDL ENTITY and ARCHITECTURE construct.
      10 Marks

END OF ASSIGNMENT